be ignored, switching speeds for GaAs and silicon will be similar for comparably designed structures operated at high-bias levels. (This latter conclusion ignores differences in parasitic contributions.) At low-bias levels, scaling principles indicate the silicon delay times will be longer than those of gallium-arsenide by the ratio of their mobilities. Intermediate fields will result in shorter delay times for gallium-arsenide.

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A MESFET Model for Use in the Design of GaAs Integrated Circuits

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Abstract—**A MESFET model is presented that is suitable for use in conventional, time-domain circuit simulation programs. The parameters of the model are evaluated either from experimental data or from more detailed device analysis. The model is shown to be more complete than earlier models, which neglect transit-time and other effects. An integrated circuit (IC) design example is discussed.**

I. Introduction

THE PURPOSE of this paper is to present a reasonably simple analytical model for the GaAs MESFET that is appropriate for use in circuit simulation programs. A number of presently available models will be reviewed and criteria for accurate modeling will be presented. Several examples of logic circuit simulation will be described.

The design and development of GaAs integrated circuits (IC's) is aided considerably if circuits may be studied using high-speed computers. Many large computer programs are available for studying dc and transient characteristics of complex combinations of transistors, resistors, capacitors and inductors. However, the success of the mathematical simulation depends totally on the accuracy of the mathematical model. The model must reflect the exact physical properties of the circuit.

The difficulty with MESFET devices is that they are extremely complex internally and simple external models cannot accurately describe their behavior under all conditions. Conversely, a detailed two-dimensional (internal) model [1]–[4] of the device, although more accurate, is not suitable for use with circuit simulation programs.

One approach is to then develop an external characterization of the particular MESFET devices used in the circuit under study. That is, the model used will not attempt to be complete enough for all ranges of device parameters.

A number of MESFET models can be found in the literature. Madjar and Rosenbaum [5] utilize the two-dimensional model of Yamaguchi and Kodera [3] to produce analytical relationships for drain and gate currents as a function of drain–source voltage, gate–source voltage, and their derivatives. This approach appears useful for studying the interaction between the device with its parasitics and its external circuits, such as in frequency multiplier operation. However, the technique would not

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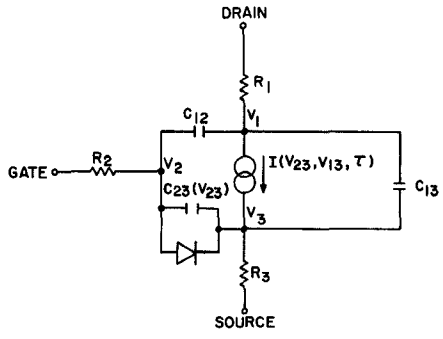

Fig. 1. Circuit model of a GaAs MESFET for use with a circuit analysis program.

be practical in the simulation of circuits with multiple-interacting devices.

Rauscher and Willing [6] have simulated FET amplifiers and oscillators in the time domain with a nonlinear-circuit-type model that includes elements representing the high field domain. Values for the linear and nonlinear elements are determined from S-parameter measurements at many bias conditions. The elements with essentially bias-independent values are considered linear. The model has not been applied for circuits with multiple FET's.

A simplified analytical model has been formulated by Shur [7]. He has used Shockley's equations and the assumption that current saturation occurs due to the formation of a stationary Gunn domain at the drain side of the gate when the average electric field under the gate equals the domain sustaining field given as: $v_s/\mu(v_s$ is the saturation drift velocity, μ is the low field mobility). The MESFET equivalent circuit is similar to the circuit to be described here; however, electron transit time effects under the gate have been omitted.

The JFET model in SPICE 2 [8] is widely available for circuit simulation studies. However, this model has several deficiencies when applied for GaAs MESFET's. As will be shown, this model is quite in error with regard to drain current–voltage relationships below current saturation. Furthermore, electron transit-time effects under the gate are omitted.

The most complete analytical model is presented by Van Tuyl and Liechti [9]. It is similar to the model to be described here but is slightly more complicated. Computer simulation of a MESFET frequency divider operating at 2 GHz showed excellent agreement with experimental data [10].

Pucel *et al.* [11] present a small signal model and show how to derive the element values. Krumm *et al.* [12] use a similar model but include electron transit-time effects as a time delay factor associated with the drain current source. Good agreement is shown for S-parameter data over a broad frequency range (2 to 18 GHz). A MESFET circuit model for transient simulations should not be very different than those models verified for small signal operation in the frequency domain.

Fig. 1 is the proposed large-signal model for the GaAs MESFET. It consists primarily of a voltage-controlled current source $I(V_{23}, V_{13}, \tau)$, three interelectrode capacitors, and a clamping diode between gate and source. Resistors R_1, R_2, and R_3 represent resistance of the contact regions. The only nonlinear elements are $I(V_{23}, V_{13}, \tau)$ and $C_{23}(V_{23})$. The important aspects of the evaluation of these elements will now be described.

II. Properties of an Accurate MESFET Model

The properties that an MESFET model must contain for accurate transient simulation will now be reviewed.

A. Accurate Approximation to the Drain Current Control Characteristics

The drain current relationship to drain–source voltage and gate–source voltage is usually known either from experimental measurements of test devices or from detailed device calculations. The MESFET model must use analytical expressions to approximate this relationship. Often several parameters are required and must be determined by curve fitting techniques. Analytical analysis of the symmetrical JFET model (see Sze [13]) results in a (gate) voltage-controlled drain current source (in the current saturation region) of the form

$$I_{DS} = I_p \left[1 + \frac{V_{GS} + V_{BI}}{V_p} \right]^N \tag{1}$$

where I_p is the "pinch off current" as defined by Sze and more commonly called saturation current, V_p is the pinch off voltage which is $qN_0a^2/(2\epsilon)$ for uniform doping, V_{BI} is the built in voltage at the gate (a negative voltage), V_{GS} is the gate–source voltage, a is the active layer thickness, and N_0 is the donor value. N is found to vary between 2.0 and 2.25, depending upon the charge distribution assumed. It will be seen that the square-law assumption is quite good for real devices.

A second form of control characteristic assumed by Fair [14] and others is

$$I_{DS} = I_p \left[1 - \sqrt{\frac{|V_{GS} + V_{BI}|}{V_p}} \right]. \tag{2}$$

This equation is also used only in the region of current saturation. This form is obtained by assuming that the depletion thickness is the same as that obtained in an abrupt junction, or

$$\sqrt{\frac{|V_{GS} + V_{BI}| \cdot 2\epsilon}{q \cdot N}} \quad . \tag{3}$$

The current is proportional to the conduction channel width which is "a" less expression (3). By using the definition of pinchoff voltage V_p, equation (2) can be derived for the case of uniform doping.

Equations (1) and (2) may appear to be quite different; however, in most cases, either one may be used to describe experimental devices. This can be seen by the following illustration. Assume a MESFET exactly follows (2). Fig. 2 is a graph of $\sqrt{I_{DS}/I_p}$ as a function of $(V_{GS} + V_{BI})/V_p$. Notice that it is nearly a linear function between

ordinate values of 0.1 and 0.9. Fig. 2 shows a straight line approximation, which has the equation

$$I_{DS}=0.8\,I_p\left[1+\frac{V_{GS}+V_{BI}}{1.25\,V_p}\right]^2. \tag{4}$$

This straight line approximation results in less than 2 percent (of I_p) error in the evaluation of current for ordinate values between 0.1 and 0.9. Equation (4) is just equation (1) with $N=2$ and I_p and V_p multiplied by constants. These constants have no physical significance since I_p and V_p would be determined from experimental data for $I_{DS}(V_{GS})$.

The must serious difference between the straight line approximation and (2) occurs near pinchoff, where current is quite small. Usually, this introduces little error.

Equation (1) can be put in a standard form as

$$I_{DS}=\beta(V_{GS}+V_T)^2 \tag{5}$$

where V_T is the threshold voltage measured from gate to source $V_T=V_p+V_{BI}$, and $\beta=I_p/V_p^2$.

Equation (5) is the form used in the general circuit analysis program SPICE 2. β and V_T are determined by plotting $\sqrt{I_{DS}}$ versus V_{GS}. If actual experimental values of I_{DS} are used, then a current source without source resistance is being described. To develop the model of Fig. 1, the raw data must first be processed to remove the effects of R_1 and R_3. This can easily be accomplished once the values of R_1 and R_3 are determined either by measurements [15] or by calculations. Since the voltage drop across R_3 is typically not negligible, the presence of R_3 usually has a major effect.

The current saturation in GaAs MESFET's occurs at lower voltages than in silicon devices because of the much larger low field mobility. This results in a much stronger current saturation effect. Van Tuyl and Liechti [9] point out that the hyperbolic tangent function provides a good analytical expression for current saturation in GaAs. In addition, one also wants to be able to describe drain–source conductance effects. This is not adequately described by adding a shunt resistor across $I(V_{23}, V_{13}, \tau)$ because current pinchoff is lost. The expression used in SPICE 2 seems to fit experimental devices quite well in the region of current saturation. However the fit is quite poor below current saturation. The expressions used in SPICE 2 are derived from the FET model of Shichman and Hodges [15] and are (for $V_{13}>0$)

$$I(V_{23},V_{13})=\begin{cases}0, & V_{23}+V_T<0\\ \beta(V_{23}+V_T)^2(1+\lambda V_{13}), & 0\leqslant V_{23}+V_T\leqslant V_{13}\\ \beta V_{13}[2(V_{23}+V_T)-V_{13}](1+\lambda V_{13}), & 0<V_{13}\leqslant V_{23}+V_T\end{cases} \tag{6}$$

where

$$V_{23}=V_2-V_3$$
$$V_{13}=V_1-V_3$$

and β and λ are constants.

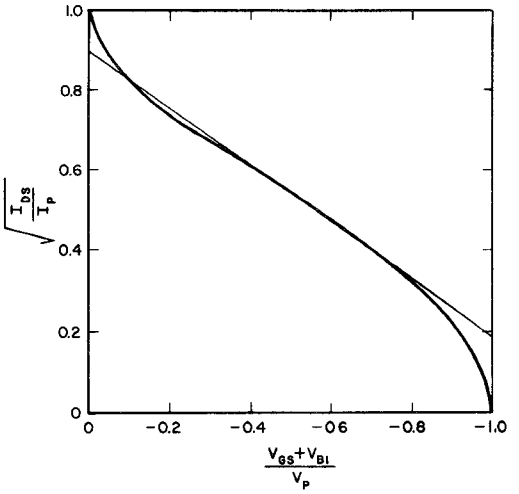

Fig. 2. Value of $\sqrt{I_{DS}/I_p}$ as a function of gate–source voltage for FET devices obeying (2).

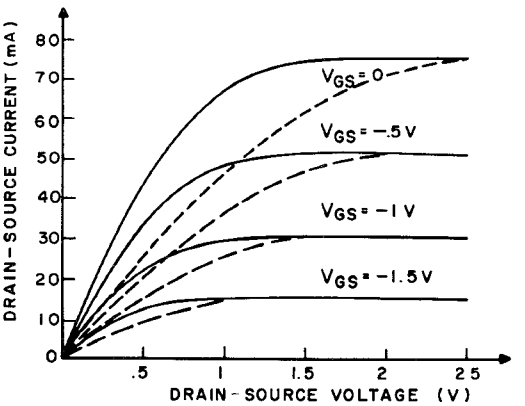

Fig. 3. Best-fit approximation to experimental MESFET I–V characteristics of [8] using the current source described by (7)—(solid lines) and by the JFET model of SPICE 2—(dashed lines). Constants are $R_1=R_3=3\ \Omega$, $\alpha=2.3\ V^{-1}$, $\beta=13.1$ mA, $V_T=2.63$ V, $\lambda=0$.

The use of the hyperbolic tangent function greatly improves the usefulness of the equation below saturation. The following analytical function is proposed for description of the current source in GaAs MESFET's:

$$I(V_{23},V_{13})=\beta(V_{23}+V_T)^2\cdot(1+\lambda V_{13})\tanh\alpha V_{13} \tag{7}$$

where α and λ are constants. Notice that there are four parameters to be evaluated in this expression.

Equation (7) was used to approximate a set of measured drain current–voltage relationships presented by Van Tuyl and Liechti [9]. The experimental data can be matched quite accurately. Fig. 3 shows the characteristics calculated from (7). For comparison purpose, the JFET model of SPICE 2 (6) was also used and these computations are shown in Fig. 3 as dashed lines. Notice that although the gate control is accurately given by both models in the region of current saturation, the SPICE 2 calculations are quite in error below current saturation due to the lack of a parameter to adjust the saturation point. This is a major deficiency of the SPICE 2 model and leads to significant error in computations of switching characteristics.

Equation (7) was also used to approximate the experimental data presented by Pucel *et al.* [11] for a 1-μm MESFET with current voltage characteristics quite different than the previous case. Fig. 4 shows the drain–source characteristic calculated from the model with the parameters listed and the experimental points are also indicated. It is seen that this simple model with analytic current expression provides a good approximation to the experimental device's current–voltage characteristic.

B. Inclusion of Transit-Time Effects

During transient operation, a change in gate voltage does not cause an instantaneous change in drain–source conduction current. This results because in order for conduction current to change, the electron depletion width under the gate must be changed and this occurs by charge transport at a maximum velocity of 1×10^7 cm/s. Thus, it takes of the order of 10 ps for a change in current after the gate voltage is changed in a 1-μm gate length MESFET. (Notice that in the physical device, this charge change is part of the gate capacitance change whereas in the model, we have separated the capacitance and current effects.) The most important result of this effect is a time delay produced between gate–source voltage and drain current. Therefore, the current source (7)

$$I[V_{23}(t), V_{13}]$$

should be altered to be

$$I[V_{23}(t-\tau), V_{13}]$$

where τ is equal to the transit time under the gate.

The time delay effect is not easily added to most circuit analysis programs. We have found a technique that accurately approximates the effect but is simple to calculate. The current source is assumed to be of the form

$$I(V)-\tau\frac{dI(V)}{dt} \tag{8}$$

where the derivative is evaluated as

$$\frac{dI(V)}{dt}=\left[\frac{\partial I(V)}{\partial V_{23}}\right]_{V_{13}}\cdot\frac{dV_{23}}{dt}. \tag{9}$$

The second term in expression (8) is a correction term which may be thought of as the first term of the expansion of $I(t-\tau)$ in time. An error is generated when the gate-to-source voltage has a nonzero second derivative. However, for small values of τ, the error is quite small. In addition, the gate's capacitance helps smooth voltage changes.

Fig. 5 shows the drain current calculated for a 1-μm MESFET device with constant drain–source voltage (3 V) and a gate voltage change from -0.5 V to $+0.5$ V in 100 ps. The current delay seen for the case of $\tau=0$ is produced by the time involved in charging the gate capacitance. The current delay seen for the case of $\tau=10$ ps is the total delay through the device. Here it is seen that there is some compromise at the beginning and end of the output current waveform but the majority of the waveform is properly time shifted by 10 ps. Fig. 5 shows that if τ is not included at all, then an important source of delay in any MESFET circuit is omitted.

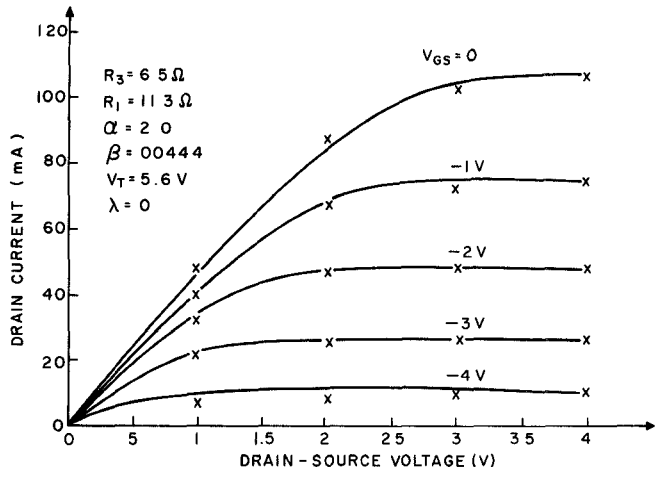

Fig. 4. Best-fit approximation to experimental MESFET I–V characteristics (X) of [10] using the current source described by (7)—(solid lines).

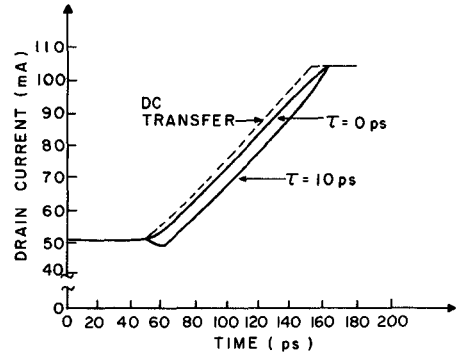

Fig. 5. Calculated drain current as a function of time for a 1-μm gate length MESFET (500-μm width) for a gate-voltage change from -0.5 to $+0.5$ V in 100 ps with delay time τ as parameter and $V_{DS}=3.0$ V. Constants are same as in Fig. 3 and $C_{23}(0)=0.5$ pF, $C_{12}=0.03$ pF, $C_{13}=0.1$ pF, $V_{BI}=1.0$ V, $R_2=10\ \Omega$.

There will also be some transit-time effect produced by drain–source voltage changes if there is a corresponding change in drain–source current. This effect should only be significant for drain–source voltages below current saturation and is not presently accounted for in this model.

The proposed model includes transit-time effects in driving transistors and in source-follower transistors but not in transistors used for active loads since $dV_{23}/dt=0$. A MESFET logic circuit would use all three types of operation (see Van Tuyl and Liechti [9]).

C. Accurate Evaluation of Gate Capacitance

The charge depletion region beneath the gate produces gate capacitance between the gate and the source C_{23} and between the gate and the drain C_{12}. Each capacitor may be thought of as a Schottky-barrier diode with voltage dependent capacitance. For a negative gate–source voltage and small drain–source voltage, each diode is back biased about the same amount and the capacitances C_{12}

and C_{23} are about equal. However, as the drain–source voltage is increased, more depletion exists on the drain side of the gate compared to the source side and C_{12} becomes smaller than C_{23}. When drain–source voltage is increased beyond the point of current saturation, C_{12} is much more heavily back-biased than C_{23}, and the charge depletion region even extends well out from the gate toward the drain. In the case $C_{12} \ll C_{23}$. These observation have been made by study of the results of the two-dimensional simulation of MESFET's.

Since the voltage drop between the source and the conductive region beneath the gate is always small, the gate–source capacitance C_{23} is usually significant and dominates the input impedance of the MESFET. For many MESFET devices, this capacitance varies much like a simple Schottky-barrier diode capacitance. This capacitance can be easily measured as a function of gate bias with or without drain–source bias. In the model of Fig. 1, drain–source bias should be used while capacitance is being measured. The voltage V_{23} must be determined from V_{GS} knowing R_3.

An analytical expression of the form derived for an ideal metal–semiconductor junction (17) is usually able to approximate such data; such as

$$C_{23}(V_{23}) = \frac{C_{23}(0)}{\sqrt{1 - V_{23}/V_{BI}}} \tag{10}$$

where V_{BI} is the built in voltage. However, the denominator must not be allowed to approach zero as V_{23} approaches V_{BI}. The capacitance will increase as the depletion width reduces and as a forward bias condition occurs, diffusion capacitance will become important. Approximation of this condition may be important for enhancement-type MESFET's.

The built in voltage V_{BI} should be evaluated experimentally from capacitance data. It should be equal to the built-in voltage of the Schottky-barrier junction pulse some part of the voltage drop along the conducing channel under the gate.

It is interesting that (10) which is derived from a two-terminal model is a good approximation for the three-terminal MESFET. The reason seems to be that the gate–source capacitance is a very weak function of drain–source voltage, once current saturation has occurred (in MESFET's not exhibiting domain effects). As the drain voltage is increased (above the voltage of current saturation) the voltage in the conducting channel beneath the gate changes little and there is an increased voltage drop across the conducting region between the gate and drain.

A two-dimensional transient simulation of a typical 1-μm gate length MESFET was used to study the gate–source and gate–drain capacitance due to internal space charge. This analysis is quite similar to that presented by Yamaguchi *et al.* [3] and Wada and Frey [4] and is an extension of the two-dimensional modeling technique described by Curtice [18]. Both C_{13} and C_{23} can

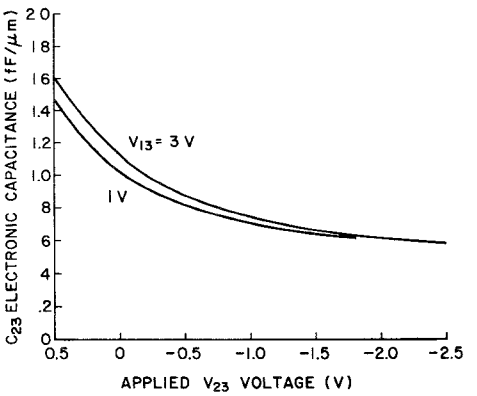

Fig. 6. Electronic gate–source capacitance as a function of gate–source voltage V_{23} and drain–source voltage V_{13} calculated from the two-dimensional model for a 1-μm GaAs MESFET with donor density $= 7 \times 10^{16}/\text{cm}^3$ and epilayer thickness $= 0.25$ μm.

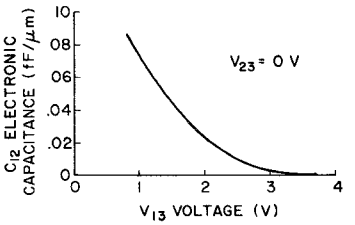

Fig. 7. Electronic drain–gate capacitance as a function of drain–source voltage V_{13} calculated from the two-dimensional model for a 1-μm GaAs MESFET with donor density $= 7 \times 10^{16}/\text{cm}^3$ and epilayer thickness $= 0.25$ μm.

be studied for a given device structure using the two dimensional simulation. Some results are presented in Figs. 6 and 7 for a uniformly doped device of $a = 0.25$ μm and donor density $= 7 \times 10^{16}/\text{cm}^3$ Field-dependent diffusion is included and V_{BI} is taken to be 0.5 V.

The gate–source capacitance is evaluated from the total change flow due to gate displacement current produced by a charge in gate-to-source voltage. Gate–drain capacitance is found from gate displacement produced by a change in drain–source voltage.

Fig. 6 shows that there is little change in the gate–source capacitance as a function of internal drain–source voltage V_{13} above current saturation. But observe that the voltage drop across R_3 may cause a change in gate–source capacitance as the external drain–source voltage is changed if there is significant change in drain current (due to finite drain resistance).

Fig. 6 also shows good agreement with (10). However, the value of V_{BI} that must be used is that due to the Schottky barrier junction *plus* a contribution of about 0.5 V apparently due to the voltage drop in the conduction channel under the gate.

The calculated values of gate–drain capacitance were quite small but increasing with reduction of drain–source voltage, as shown in Fig. 7. As we shall see in the next section, the electrostatic capacitance between gate and drain will usually be much larger than these values. However, if calculations or measurements show that C_{12} is an important voltage-variable capacitance, then it must be

included in the model. Willing *et al.* [19] present data for such a case. This effect is not related to the Miller effect, which is fully included when simulation is performed with loading on the MESFET.

When the active layer thickness and donor value are large enough, in stationary charge accumulation region can exist beneath the drain edge of the gate and just above the substrate interface. The charge accumulation region together with the charge depletion region adjacent to it on the drain side form the stationary high-field domains reported by Yamaguchi *et al.*, Wada and Frey, and others. For the device studied here, only a small amount of charge accumulation is present and only for the case of near zero gate–source bias voltage. If the domain is present over much of the operating range of the device, the interelectrode capacitances may be affected as well as the current control characteristics. The gate–drain capacitance is increased due to the smaller depletion region and the gate–source capacitance may become a strong function of the drain–source voltage as well as the gate–source voltage. Willing *et al.* [19] show such a case. Such domain effects can be important in power MESFET's but are usually less important in devices used in integrated circuit that are typically of lower donor-thickness product [20].

D. Evaluation of "Nonelectronic" Drain–Gate and Source–Gate Capacitances

Experimental drain–gate and source–gate capacitances depend very little upon the operating biases. They are determined primarily by the electrostatic coupling between parallel conductors, quite independent of the internal space charge distribution. From exact solutions of the simplified theoretical problem, Pucel *et al.* [11] have calculated and plotted the drain–gate and source–gate capacitances as functions of electrode separation. Gate length is a parameter for drain gate capacitance and source (or drain) length is a parameter for source–drain capacitance. The geometry is planar and no ground plane is present. The authors state that the source–drain capacitances are in good agreement with experimental measurements whereas the drain–gate capacitances are somewhat higher than the experimental values. Typical values for gate–drain and drain–source capacitance are thus 0.1 fF/μm and 0.15 fF/ωm, respectively.

E. Evaluation of Circuit Parasitics

As the MESFET circuit is made smaller, the pad capacitances and other parasitics become more important. For example, the capacitance-to-ground of the drain contact of a driver transistor can cause significant loading. The metal line providing signal transmission between logic gates of an IC can also introduce capacitive loading effects to ground and also capacitive coupling (or mutual capacitance) effects to other signal transmission lines.

There are several methods of estimating the fringe capacitive effects of a particular IC layout. Maupin *et al.* [21] have computed the complete capacitance matrix (i.e., interelectrode capacitances and capacitances to ground) for the metal contact pads (source, gate, and drain) of each MESFET type and in their circuit. This computation is done by theoretical analysis assuming a ground plane under the substrate.

A second method is to build scaled-up models of the MESFET circuits and to measure interelectrode capacitance and capacitances to ground. VanTuyl *et al.* [10] define metal layouts 10 times actual size and on sapphire substrates. A standard capacitance bridge is used. Excellent agreement with theoretically computed values of capacitance of simple shapes was found. This technique has enabled them to reduce their propagation delay through reduction of parasitic capacitances with improved layout designs.

A dramatic example of the importance of circuit parasitics is presented by VanTuyl, Liechti *et al.* [10],[22]. They show that for a given circuit layout, the propagation delay of a gate is equal to a constant plus a term inversely proportional to transistor width. These two terms become equal at a (buffer) transistor width somewhat less than 10 μm. At this point, the parasitics have doubled the inherent delay of the gate.

III. Dual-Gate FET Modeling

The dual-gate MESFET structure must also be modeled since it is useful for performing ANDing. Asai *et al.* [23] showed that the dual-gate device behaves similar to two FET's in series with each device somewhat inhibiting the operation of the other.

Fig. 8 shows the equivalent circuit assumed for simulation of the dual-gate device. The two equivalent FET's, designated as FET 1 and FET 2 in the figure, consists of a voltage-controlled current source and a voltage-variable gate capacitance as described in Section II.

The saturation current of the dual-gate device is less than that of a single-gate FET. In addition, the g_m of the second gate is lower than the g_m of the first gate because the second device (FET 2) has the first device (FET 1) as a source resistance.

To help offset these effects, the second gate section of the device is usually made 25 to 50 percent wider than the first gate. Fig. 9 shows how the calculated saturation current of the device changes with the width ratio. This calculation assumes parameters typical of a 1-μm gate length MESFET. The width at FET 1 is 500 μm. In addition to lower current, the dual-gate FET has a higher "knee" voltage, i.e., current saturation occurs at a larger drain–source voltage.

To observe the transient response of the dual-gate device, a logic gate was simulated with two dual-gate FET's in parallel as drivers. This is the equivalent of two 2-input NAND gates feeding an OR gate. A width ratio of 1.5 was used for both FET's and the fanout was assumed to be unity. Table I shows the calculated propagation delays for switching with either gate and for an equivalent single gate driver. The relationship of the numbers is quite similar to the measurements by Van Tuyl *et al.* [10]. This

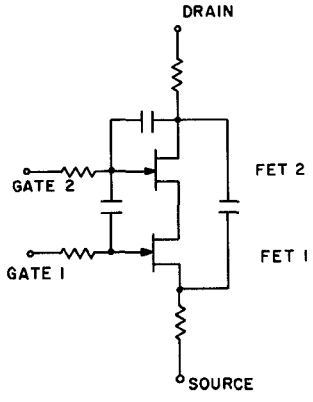

Fig. 8. Equivalent circuit for the dual-gate MESFET.

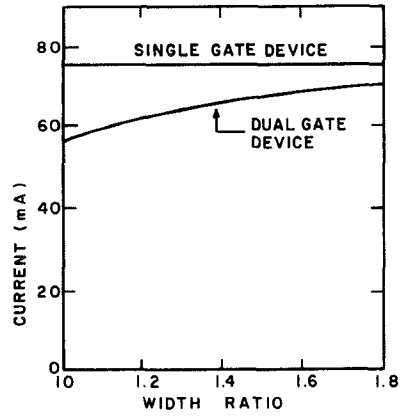

Fig. 9. Saturation current of the dual-gate MESFET as a function of the width ratio at the gates. Constants are same as in Fig. 3 and $V_{GS}=0$.

TABLE I

CALCULATED PROPAGATE DELAYS FOR NAND/NOR GATE

	Propagation Delay (ps)
Using Upper Gate:	80
Using Lower Gate:	87
Using Single Gate FET:	67

is thus good justification for the model. In addition, it is clear that there is a significant increase in the propagation delay for dual-gate devices as compared to single-gate FET's.

IV. SIMULATION EXAMPLE

The model shown in Fig. 1 may be used with a circuit simulation program to study complex integrated circuits. The circuit simulation program used here is R-CAP(24). It is similar to SPICE 2 in many respects but has the advantage that a user-defined device model can be included without difficulty. The model for the GaAs MESFET was added to R-CAP as a subroutine.

The first circuit example is a MESFET amplifier with nonlinear load and is shown in Fig. 10. This circuit is a logic gate without the level-shifting stage. Assuming certain device parameters, the circuit was simulated using R-CAP, SPICE 2 and also by the two-dimensional modeling program. The individual device characteristic were

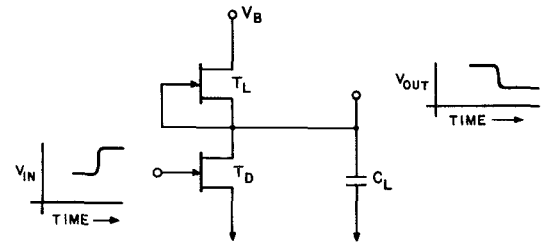

Fig. 10 MESFET logic gate without the level-shifting circuit. MESFET T_L is the same but one-half the width of MESFET T_D.

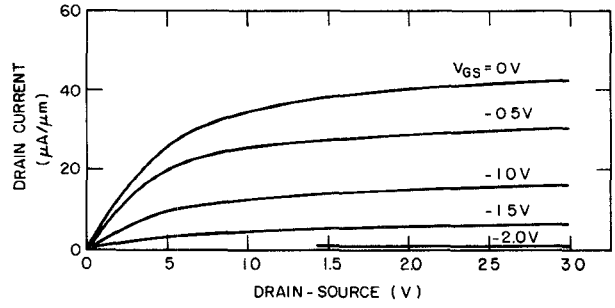

Fig. 11. Drain–source current–voltage relationship for a GaAs MESFET calculated by the two-dimensional program assuming gate length = 1.0 μm, donor value = $3\times10^{16}/cm^3$, active layer thickness = 0.25 μm, built-in voltage = 0.5 V.

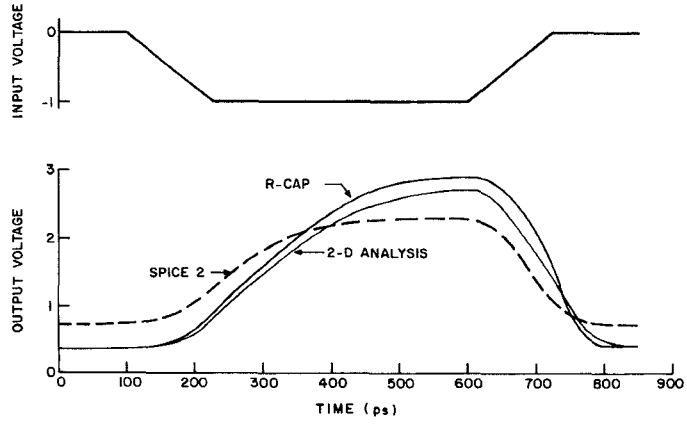

Fig. 12. Comparison of simulation results using R-CAP, SPICE 2 and the two-dimensional analysis for the device of Fig. 11 with $V_B=3.5$ V and for SPICE 2: $V_T=2.5$ V, $\beta=71$ μA/V², $\lambda=0$, $V_{BI}=0.5$ V, $C_{23}(0)=6$ fF, $C_{12}(0)=1$ fF, for R-CAP: $\alpha=1.5/V$, $\beta=65$ μA/V², $V_T=2.5$ V, $V_{BI}=0.5$ V, $C_{23}(0)=6$ fF, $C_{12}=0.3$ fF, $\tau=10$ ps. For Both: $R_1=R_2=R_3=C_{13}=0$, $C_L=6$ fF, driver width = 10 μm, load width = 5 μm.

first calculated from the two-dimensional program assuming 1-μm gate length, a donor value of $3\times10^{16}/cm^3$, an active layer thickness of 0.25 μm, and a built-in voltage of 0.5 V. The calculated drain–source current–voltage characteristics are shown in Fig. 11. The parameters necessary for SPICE 2 and R-CAP were than evaluated. Fig. 12 shows the results of circuit simulation by the three methods for a specific input (gate) voltage waveform. The two-dimensional result is taken to be the most exact. It can be seen that the result from SPICE 2 has errors in risetime, gain and propagation delay whereas the result using R-CAP is reasonably accurate. For example, the

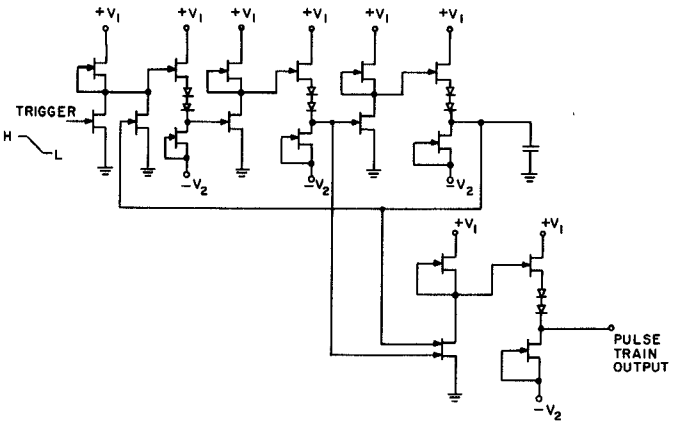

Fig. 13. Circuit design for a MESFET short-pulse generator.

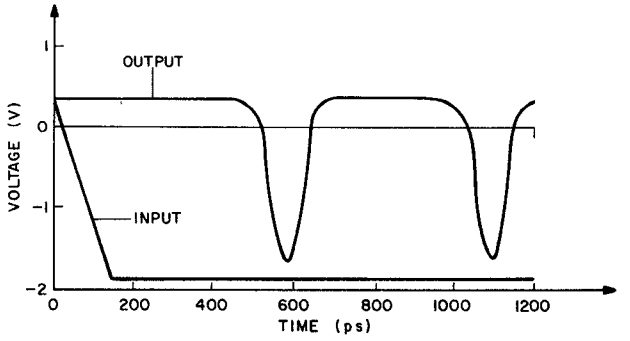

Fig. 14. Calculated output voltage as a function of time for MESFET pulse generator of Fig. 13 with $V_1=4$ V, $V_2=3$ V; MESFET. Constants are $\lambda=0$, $\alpha=2.3$ V^{-1}, $V_T=2.63$ V, $\beta=26.3$ $\mu A/\mu m$, $R_1=R_3=0.15$ $\Omega/\mu m$, $R_2=0.5$ $\Omega/\mu m$, $\tau=10$ ps, $V_{BI}=1.0$ V, FET widths: Drivers=100 μm, Load=75 μm, source follower=100 μm, source follower load=75 μm, dual-gate FET widths: lower=100 μm, upper=150 μm, load capacitor=0.5 pF, $C_{12}=0.06$ $fF/\mu m$, $C_{13}=0.2$ $fF/\mu m$.

gain predicted by SPICE 2 is 1.59 whereas R-CAP predicts 2.53 and the two-dimensional result is 2.38. The error in propagation delay for SPICE 2 is primarily related to the neglect of transient-time effects and the error in gain is due to the inability of the JFET model (in SPICE 2) to approximately the sharply saturating current–voltage characteristics of Fig. 11.

The second example is an IC design capable of producing triggerable bursts of short pulses. The goal was a half-width of 100 ps and MESFETs with a gain–bandwidth product of 15 GHz were to be used. The design developed is a triggerable ring oscillator with a NAND gate connected across two stages. Fig. 13 illustrates the circuit.

Fig. 14 shows the output pulse train as calculated by the R-CAP simulation program. It is seen that the final pulse width is about 77 ps which is well under the design goal of 100 ps. In addition, the circuit's output is not broadened by triggering with a slow input step, as shown. This is due to the high gain achieved by the FET inverter gates. The pulse train can be stopped by returning the input voltage to the high state.

The effect upon the output waveform produced by degradation of the individual MESFET's can be easily studied by further simulation.

V. Conclusion

A circuit model for the GaAs MESFET for use with time-domain circuit simulation programs has been described. The importance of accurately describing the drain current control characteristics, transit-time effects, gate capacitance, and circuit parasitics has been discussed. The parameters for the model must come from experimental measurements or from accurate detailed models, such as a two-dimensional internal model.

To illustrate the use of the model, an IC circuit design was simulated. It was shown possible to produce short pulses of less than 100 ps in a triggerable manner with an MESFET circuit. Such a circuit would be useful for timing purposes.

Acknowledgment

The author is particularly indebted to V. Alwin of the Design Automation group, SSTC, Somerville, NJ for his assistance in the use of R-CAP and the development of the user-defined model.

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Intrinsic Response Time of Normally Off MESFET's of GaAs, Si, and InP

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Invited Paper

***Abstract*—A response time of normally off MESFET's for high-speed logic circuits made of GaAs, Si, and InP was calculated using a two-dimensional numerical analysis. The results indicate that GaAs is the best material among them. The step response of the InP FET is not as fast as expected from v/E characteristics due to low electric field in the channel for low-power logic operation of a normally off FET.**

I. Introduction

RECENTLY, GaAs MESFET's have been actively used for high-speed logic circuits. Using a normally on FET, a propagation delay per gate (t_{pd}) of 34 ps with a dissipation power (P_{dis}) of 41 mW was obtained [1]. For normally off FET's, 77 ps of t_{pd} with 977 μW of P_{dis} has been achieved [2], and 72 ps with 890 μW as the latest data [3]. From these experimental results, the superiority of GaAs to Si as basic material has been made clear. Since t_{pd} of several tens picoseconds has been achieved, it is significant to estimate an intrinsic response time (t_{int}) of the FET itself.

In this paper, t_{int} for normally off MESFET's made of GaAs, Si, and InP have been calculated using a two-dimensional numerical analysis and the results compared.

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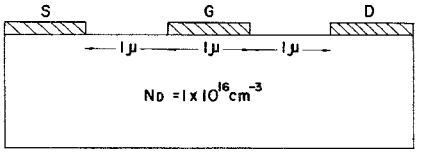

Fig. 1. The two-dimensional analytical model for MESFET.

II. Analytical Model

A model for the analysis is a two-dimensional planar type MESFET with an n-type active layer as shown in Fig. 1. For the convenience of simplicity of the calculation, a semi-insulating substrate is not considered. The donor concentration is 1×10^{16} cm^{-3}. The gate length (l_g) is 1 μm and the source–drain distance is 3 μm. Basic equations are as follows:

$$-\nabla^2\varphi = q/\epsilon\cdot(N_D - n) \tag{1}$$

$$\partial n/\partial t = \nabla(n\cdot v + D\cdot\nabla n) \tag{2}$$

$$\nabla J_{tot} = \nabla(q\cdot n\cdot v + q\cdot D\cdot\nabla n + \epsilon\cdot\partial E/\partial t) = 0 \tag{3}$$

where φ is the potential, q is the electronic charge, ϵ is the dielectric constant, n is the electron density, E is the electric field, v is the drift velocity, and D is the diffusivity. In order to solve these equations, the Successive-Over-Relaxation method was used for Poisson's equation (1) and the Successive-Under-Relaxation method was

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